UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,391	01/23/2004	Melany Ann Richmond	ZIL-555	8983

47713 7590 06/20/2007

IMPERIUM PATENT WORKS
P.O. BOX 587
SUNOL, CA 94586

EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

MAIL DATE	DELIVERY MODE
06/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,391	RICHMOND ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received April 2, 2007 for application number 10/764,391 originally filed January 23, 2004. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-23 are presented for examination.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 2, 2007 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7, 9-19 and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Bongiorno et al. (U.S. Patent No. 6,292,045 B1) (hereinafter referred to as Bongiorno).

As to claim 1, Bongiorno discloses a method comprising: (a) detecting (via 50) whether a first clock signal is inadequate, wherein the first clock signal is generated by a first clock circuit (10); (b) decoupling (via 66) the first clock circuit from a system clock input lead of a processor (80) after the detecting in (a), wherein the decoupling is not performed as a result of a signal from the processor; (c) coupling a second clock circuit (20) to the system clock input lead of the processor after the decoupling in (b); (d) enabling a third clock circuit (30) after the coupling in (c); (e) decoupling the second clock circuit from the system clock input lead of the processor after the enabling in (d); and (f) coupling the third clock circuit to the system clock input lead of the processor after the decoupling in (e) (column 2, lines 41-62 and column 3, line 52 thru column 4, line 60 and column 4, line 61 thru column 5, line 28 and column 5, line 53 thru column 6, line 35 and column 7, line 45-57; Figs. 1B and 3A).

As to claim 2, Bongiorno further discloses the method of claim 1, wherein the first clock circuit a high-speed, external crystal oscillator, wherein the second clock circuit is a low-speed, internal watchdog timer, and wherein the third clock circuit is a high-speed, internal oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-39).

As to claim 3, Bongiorno further discloses the method of claim 1, wherein the detecting is performed by detecting no signal edges of the first clock signal during a time period over which a linear feedback shift register increments to a predetermined value (Bongiorno discloses

the timer monitoring the processor clock signal such that a predetermined count value [pre-set time-out period] is incremented, as is known in the art, which can be done with or without an LFSR; column 1, lines 26-39 and column 3, line 52 thru column 4, line 21).

As to claim 4, Bongiorno further discloses the method of claim 1, wherein the second clock circuit generates a signal whose frequency is lower than that of the first clock signal, and wherein the second clock circuit and the processor are parts of a single integrated circuit (column 1, lines 11-25).

As to claim 5, Bongiorno further discloses the method of claim 1, wherein the coupling the second clock circuit in (c) is not performed as a result of a signal from the processor (Bongiorno discloses a malfunctioning clock signal being deselected from a processor after watchdog timer sends out a reset signal to the processor; therefore decoupling is performed as a result of the timer and not the processor; column 4, lines 9-21 and column 4, line 61 thru column 5, line 7).

As to claim 7, Bongiorno further discloses the method of claim 1, further comprising, between step (a) and step (b): (g) sending an interrupt signal (reset signal) to the processor indicating that the first clock circuit has failed (column 4, lines 9-21).

As to claim 9, Bongiorno further discloses the method of claim 1, further comprising, between step (d) and step (e): (g) detecting (via detector 50) whether a second clock signal is inadequate, wherein the second clock signal is generated by the third clock circuit (Bongiorno discloses the detector circuit [50] detecting the availability of the clocks that are selected; column 4, lines 22-38).

As to claim 10, Bongiorno further discloses the method of claim 1, wherein the first clock circuit can be coupled to the system clock input lead by a multiplexer, the first clock circuit being coupled to a first data input lead of the multiplexer, wherein the second clock circuit is coupled in (c) to the system clock input lead by the multiplexer, the second clock circuit being coupled to a second data input lead of the multiplexer, wherein a third data input lead of the multiplexer is grounded (inherently grounded as all circuits are grounded), and wherein between step (b) and step (c) the multiplexer couples the third data input lead of the multiplexer to the system clock input lead (column 4, line 61 thru column 5, line 7).

As to claim 11, Bongiorno discloses an integrated circuit, comprising: (a) a processor (80) with a system clock input lead (inherent that a processor chip has a system clock input lead; column 4, lines 2-8); (b) a terminal, the terminal coupled to a first clock circuit (10), the first clock circuit generating a first clock signal (element 100 is noted as an "inventive circuit" which necessitates a terminal to receive the clock from circuit 10; column 3, lines 52-57); (c) a second clock circuit (20); (d) a third clock circuit (30); and (e) a clock controller (40) coupled to the system clock input lead, wherein the clock controller is adapted to decouple (via 66) the system clock input lead from the terminal and to couple the system clock input lead to the second clock circuit upon detecting that the first clock signal has failed, and wherein the clock controller is further adapted to turn on the third clock circuit upon detecting that the first clock signal has failed (column 2, lines 41-62 and column 3, line 52 thru column 4, line 60 and column 4, line 61 thru column 5, line 28 and column 5, line 53 thru column 6, line 35 and column 7, line 45-57; Figs. 1B and 3A).

As to claim 12, Bongiorno further discloses the circuit in claim 11, wherein the first clock circuit is a high-speed external crystal oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-39).

As to claim 13, Bongiorno further discloses the circuit in claim 11, wherein the second clock circuit is a low-speed, internal watchdog timer (column 4, lines 9-15) oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-39).

As to claim 14, Bongiorno further discloses the circuit in claim 11, wherein the clock controller can decouple the system clock input lead from the terminal when the processor is receiving an inadequate first clock signal (column 1, lines 11-25).

As to claim 15 Bongiorno further discloses the circuit in claim 11, wherein the clock controller decouples the system clock input lead from the second clock circuit and couples the system clock input lead to the third clock circuit (column 3, lines 8-20).

As to claim 16, Bongiorno further discloses the circuit in claim 11, wherein the clock controller comprises a primary clock source fail detect circuit (51), and wherein the primary

clock source fail detect circuit detects whether the first clock signal has failed (is available) (column 5, lines 29-52).

As to claim 17, Bongiorno further discloses the circuit in claim 16, wherein the clock controller further comprises a secondary clock source fail detect circuit, and wherein the secondary clock source fail detect circuit detects whether a second clock signal has failed, wherein the second clock signal is generated by the third clock circuit (Bongiorno discloses the detector circuit [50] detecting the availability of the clocks that are selected; column 4, lines 22-38).

As to claim 18, Bongiorno further discloses the circuit in claim 16, wherein the clock controller comprises a plurality of substantially identical clock source fail detect circuits, and wherein each of the clock source fail detect circuits detects whether a different clock signal has failed (column 5, lines 29-52).

As to claim 19, Bongiorno discloses a microcontroller integrated circuit operable with an external first clock circuit, the microcontroller integrated circuit comprising: (a) a processor (80) having a system clock input lead (inherent that a processor chip has a system clock input lead; column 4, lines 2-8); (b) a terminal for receiving a first clock signal generated by the external first clock circuit (element 100 is noted as an "inventive circuit" which necessitates a terminal to receive the clock from circuit 10; column 3, lines 52-57); (c) a second clock circuit (20); (d) means for detecting (40) whether the first clock signal is inadequate and, upon detecting that the first clock signal is inadequate, for decoupling (via 66) the terminal from the system clock input lead and coupling the second clock circuit to the system clock input lead, wherein the means decouples the terminal from the system clock input lead and couples the second clock circuit to

the system clock input lead without receiving any signal from the processor; and (e) a third clock circuit (30), wherein the means turns on the third clock circuit upon detecting that the first clock signal is inadequate (column 2, lines 41-62 and column 3, line 52 thru column 4, line 60 and column 4, line 61 thru column 5, line 28 and column 5, line 53 thru column 6, line 35 and column 7, line 45-57; Figs. 1B and 3A).

As to claim 21, Bongiorno further discloses the microcontroller in claim 19, wherein the means decouples the second clock circuit from the system clock input lead and couples the third clock circuit to the system clock input lead after the turning on of the third clock circuit (column 5, line 53 thru column 6, line 35 and column 7, line 45-57).

As to claim 22, Bongiorno further discloses the microcontroller in claim 1, wherein the second clock circuit is a low-power, RC oscillator (column 1, lines 11-25).

As to claim 23, Bongiorno further discloses the microcontroller in claim 1, wherein the third clock circuit is entirely on-chip and does not have an external crystal (column 1, lines 11-25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno as applied to claim 1 above, and further in view of Lichter et al. (U.S. Patent No. 6,970,045 B1) (hereinafter referred to as Lichter).

As to claim 6, Lichter teaches a redundant clock module wherein the redundant clock (either 24 or 26 within 12) is enabled (powered on) when the first oscillator has failed or is "out of tolerance" (column 2, lines 28-43 and column 19-31 and column 5, lines 48-60 and column 6, lines 17-30). Lichter has the additional feature of detecting "out of tolerance" conditions in addition to failure and seamlessly switching to the redundant clock without shutdown, glitches or system crash (column 2, lines 11-24).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Lichter at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to enable (power on) redundant/back-up clock circuits when the primary clock fails or is detected inadequate as taught by Lichter. One of ordinary skill in the art would be motivated to make this combination of including the ability to enable (power on) redundant/back-up clock circuits when the primary clock fails or is detected inadequate in view of the teachings of Lichter, as doing so would give the added benefit of detecting "out of

tolerance" conditions in addition to failure and seamlessly switching to the redundant clock without shutdown, glitches or system crash (as taught by Lichter above).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno as applied to claim 1 above, and further in view of Chen et al. (U.S. Patent No. 6,816,979 B1) (hereinafter referred to as Chen).

Chen teaches a clock detection circuit wherein the clock detector can be disabled (column 4, lines 38-51). Chen has the additional benefit of detecting and resolving clock speed issues (column 1, lines 26-32).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Chen at the time the invention was made, to modify the clock switching circuit of Bongiorno to include the ability to disable clock detector when not needed as taught by Chen. One of ordinary skill in the art would be motivated to make this combination of disabling the clock detector when not needed in view of the teachings of Chen, as doing so would give the added benefit of detecting and resolving clock speed issues (as taught by Chen above).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno as applied to claim 19 above, and further in view of Triece (U.S. Patent Publication No. 2003/0079152 A1) (hereinafter referred to as Triece).

As to claim 20, Triece teaches a clock selection microcontroller wherein a means couples the system clock input lead to ground (from input 152 of multiplexor 150 or 450) after decoupling the terminal from the system clock input lead and before coupling the second clock circuit to the system clock input lead (paragraph 33, lines 15-26 and paragraph 47, lines 21-36).

Triece has the additional benefit of enabling power saving modes to be more flexible with many applications (paragraph 2).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Triece at the time the invention was made, to modify the means of Bongiorno to include a ground selection to a clock input lead as taught by Triece. One of ordinary skill in the art would be motivated to make this combination of including a ground selection to a clock input lead in view of the teachings of Triece, as doing so would give the added benefit of enabling power saving modes to be more flexible with many applications (as taught by Triece above).

Response to Arguments

Applicant's arguments filed April 2, 2007 have been fully considered but they are not persuasive.

Having taken claims, arguments and references into further consideration, the Examiner has presented new grounds of as shown hereinabove with response to arguments to discussed below.

In re claim 1, the Applicant argues that "nowhere in the cited passages above does Bongiorno teach coupling a third clock circuit after decoupling a second clock circuit after coupling the second clock circuit after decoupling a first clock circuit. Bongiorno teaches only switching to one clock from another clock" (Remarks, page 9, lines 4-7). The Examiner disagrees. Bongiorno teaches a clock controlling circuit that selects a second clock source when a first clock source has failed. In doing so, Bongiorno continues to teach that the clock sources can be selected in a priority order based upon programming code. Bongiorno shows a table

(Table 1, column 6) that represents in what order the clock sources can be selected. If code '000' is coded, then the first clock selected will be clock source 10. If clock source 10 were to fail, the next selected clock source would be clock 20. And, if clock source 20 were to fail, the next selected clock source would be clock 30 (column 6, lines 1-35). The clock selection process of coupling and decoupling is stepped out in Fig. 4 at steps 400-440 (column 7, lines 38-57). Therefore, Bongiorno ***does teach*** coupling a third clock circuit after decoupling a second clock circuit after coupling the second clock circuit after decoupling a first clock circuit. Likewise, Bongiorno ***also teaches*** "(i) deselecting a first clock source (10), (ii) then selecting a second clock source (20), (iii) then deselecting the second clock source (20), and (iv) then selecting a third clock source (30)" as argued in Remarks, page 10, lines 10-14.

In re claims 1 and 11, the Applicant argues that Bongiorno does not teach enabling or coupling a third clock circuit. The Examiner disagrees. As presented above, Bongiorno does teach selecting/coupling/enabling a third clock source (30) wherein said third clock source is selected using a switching means (66 or 660) that inherently couples and enables the selected clock source (column 4, lines 61 thru column 5, line 7 and column 5, lines 29-52).

Applicant also argues that reference Lichter does not have priority over the instant application's effective filing date. However, filing a provisional application under 35 USC § 119(e) deems the reference [Lichter] to have an earlier effective filing date than said instant application. The Applicant is instructed to refer to MPEP 706.02 for further detail.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
June 12, 2007

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
6/18/07